Screening vs. Qualification
for Microcircuits

NASA Electronic Parts & Packaging Program (NEPP)
Electronics Technology Workshop (ETW)

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The "Yellowknife Bay" formation in Mars' Gale Crater, where the Curiosity rover unlocked a trove of life-related findings.
Image credit: NASA/JPL-Caltech/MSSS

The Two Major Divisions of Parts Assurance Testing

- **(Note: Parts here is primarily monolithic microcircuits.)**

- **Parts assurance testing is mostly composed of two areas: screening and qualification**

- **Screening tests are**
  - Performed on 100% of a production lot (see 38535K, pp. 18-22)
  - A measure of product quality

- **Qualification tests (also called quality conformance inspection (QCI) are performed on a sample to guarantee the performance of the rest of the lot.**
  - Performed on **only part** of a lot (See 38535K, pp. 24-32, 116-118)
  - A measure of product reliability and radiation assurance

- **Other tests may include**
  - Destructive physical analysis (DPA)/Parts construction analysis (PCA)
  - Additional tests defined in microcircuits specification, MIL-PRF-38535, particularly in Appendix H
  - Specific tests for the project

Bathtub Curve
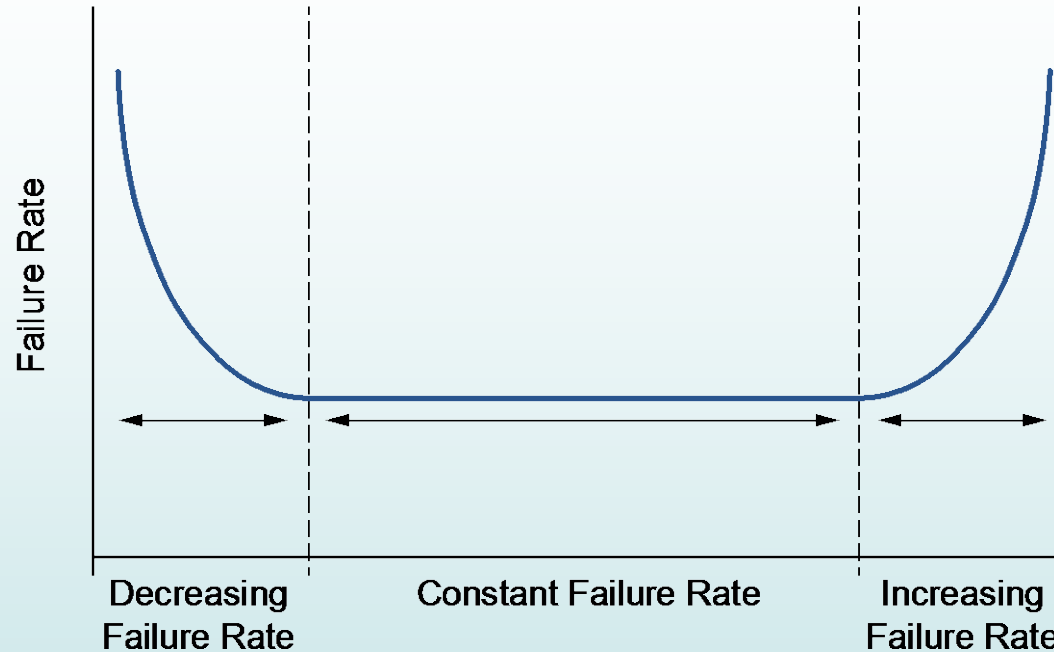
In the early life of a product, the failure rate is high but rapidly decreasing as defective products are identified and removed. In the mid-life of a product, the failure rate is low and constant. In the late life of the product, the failure rate increases, as age and wear take their toll.

Screening and Qualification

- **From the next few slides, we'll see how the screening and qualification tests go hand-in-hand.**

Example 1, Cassini Mission (Launched 1997): Testing New Products as Being Manufactured

- **Procurement overview**
  - Large procurement (e.g. high-speed silicon-on-sapphire logic from Intersil)
  - Substantial budget
  - Screening and QCI done to space flows

- **Some test related details**
  - Pre-cap inspection done by JPL QA
  - Realistic specification limits for leakage currents over temperature, radiation, life were established
  - Radiation assessment / testing
  - Destructive physical analysis (DPA) of each lot
  - Software developed to review parametric changes (deltas)
  - JPL reviewed electrical test programs and burn-in circuits

  - Worked well

- Note: Voyager 1, 2 (1977) and Galileo (1989) parts plans also required screening and qual testing.

Example 2, MER (Launched 2003): Upscreening of Plastic Encapsulated Microcircuits (PEMs)

- **Procurement overview**
  - Done for MER Cameras
  - Large quantities of each PEM function were procured
  - Parts complexity: Medium Scale Integration (MSI)
  - Sufficient budget
  - Performed both screening and qualification
- **Some test related details**
  - Glass transition temperature
  - C-mode scanning acoustic microscopy (CSAM)
  - Radiation assessment / testing
  - DPA
  - Software developed to review parametric changes
  - JPL reviewed Electrical test programs and Burn-in circuits
  - Heavy engineering effort put into data analysis

  - Worked well; no problems reported during mission

Future Screening and Qualification Possibilities

- **Automotive Parts**

- **System-on-a-chip (SOC) in Plastic Package**
  - Xilinx V-5 will be tested for MSFC's SLS project The following tests are planned:
    - ❖ DPA/PCA
    - ❖ Screening
    - ❖ QCI
    - ❖ Single Events Effects (SEE)

- **NASA-led initiatives for space parts**
  - Class Y

- **Industry-initiated new products**
  - Base metal electrode (BME) capacitors inserted in microcircuit packages
    - ❖ Screening and qualification flows being developed by an industry group

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Future Screening and Qualification Possibilities

- **Industry Initiatives (Contd.)**
  - New Technology for Aerospace
    - ❖ Infusion of future technology
  - G12 Task Group on Plastic Packages.
  - G12 Task Group on PEM qualification and screening flows
    - ❖ Avionics / Terrestrial applications
    - ❖ Space application

- **NESC-RP-12-00759, February 27, 2014**
  - NASA has a part policy directive in NPD 8730.2 and no Agency-level parts requirements (NPR).
  - Parts requirements are defined at Center-level and project-level, such as
    - ❖ EEE-INST-002,
    - ❖ MSFC-STD-3012
    - ❖ (The above documents address screening and qualification of parts.)

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Example 3, Evaluation of Automotive Microcircuits

- **Existing automotive parts market**
  - Plastic packages
  - No screening is done
  - Much testing is done at the wafer level
  - Limited qualification
  - The customer must enforce any desired requirements
  - Manufacturers self certify—no DLA-type regulators
  - The system works because of **high-volume production**—That is the customer's power to enforce upgrades

- **Evaluation is in progress (2014)**
  - Refer to automotive parts presentation
  - Screening and qualification are planned
    - ❖ Tight budget
   - ❖ Qualification will be limited to life test

Issues for Screening and Qualification of New Parts

- **Often, funding is <u>not unlimited</u>**

- **Negotiating requirements between the user community and the manufacturers**

- **Finding the best fit for project needs**

- **Introduce new ways of specifying requirements**
  - Example: Package Integrity Demonstration Test Plan (PIDTP); post column electricals for Class Y in MIL-PRF-38535, Rev. K

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Infrastructure Development for Microcircuits

- QML/QPL Monolithics and Hybrids
  - Qualified Manufacturer Listing / Qualified Parts Listing.
  - Program is administered by the Defense Logistics Agency (DLA) Land and Maritime, Columbus, Ohio.
  - Technical support provided by NASA, the Aerospace Corporation and others

- Upscreening
  - Done at user's risk. Upscreening flow developed by parts specialist. Evaluate for radiation.
  - Examples: Q to Q+; upscreening of PEMs.

- Infusion of new technology into DoD standards
  - By manufacturers: Dual use technology
  - Led by NASA for space community: Class Y
  - Path for future Nano products

- Other
  - Automotive Parts: under evaluation by a NASA/Navy team
  - COTS:– being addressed by an NESC team
  - NASA meeting on parts for small missions
  - NASA ETW
  - Medical Electronics: under evaluation

- Use of Commercial Parts as-is
  - Consult parts specialist
- Board-level issues
  - Testing
  - Heat removal/power management
- Some Issues with COTS
  - Reliability of Copper wires (JEDEC)
  - Hot spots (JEDEC)
  - Reported screening failures: 3% reported on Commercial FPGAs (24 failed out of 800 tested)
  - NASA will have its own data soon.

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Bathtub Curve and Feature Sizes
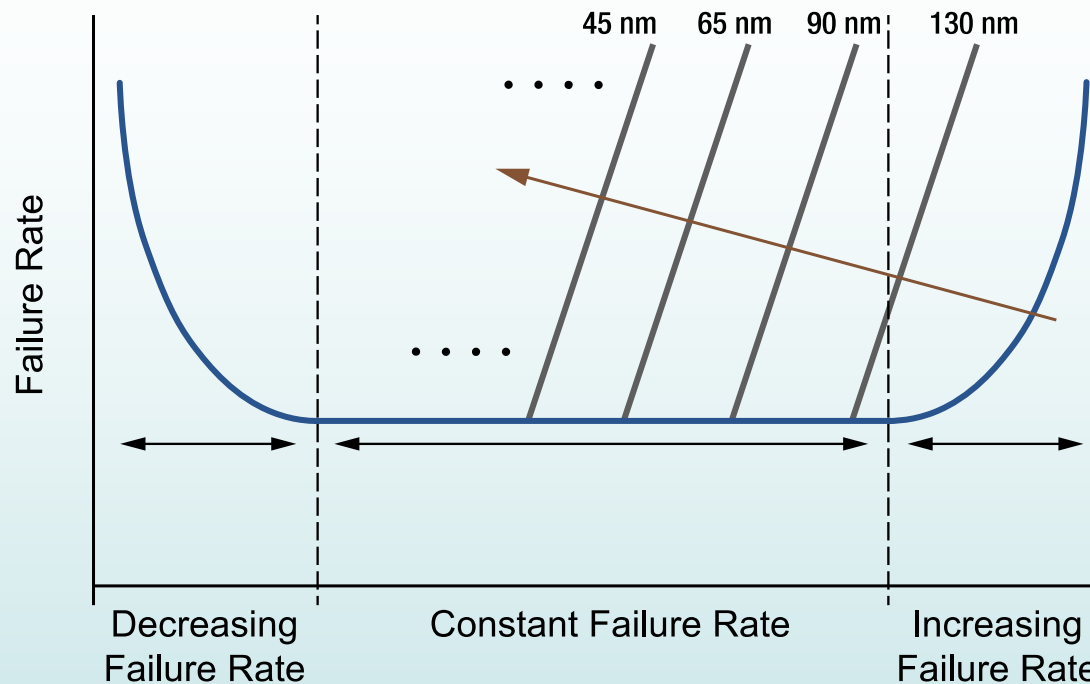
It has been reported that as the feature sizes get smaller, the product useful life gets shorter. Should be further investigated if considering use of COTS with small features, particularly below 45nm (e.g., 35nm, 28nm, 20nm, 14nm).

Burn-in (BI)

- **BI is the key screening step** – considered essential to weed out product infant mortality.
- BI circuit is also used for reliability testing – life test (QCI, Group C)
- Our recent audit and specification review work has shown that the microcircuits BI screening requirements as stated in MIL-STD-883, Test Method 5004, are **out of date and have multiple interpretations**.

- **Why are they out of date?**
  - Were developed more than 25 years ago
  - Then: were at 5-micron technology node
  - Now: 45-nm space products in development, on their way to QMLV certification. Made possible by
    - ❖ Dual-use technology
    - ❖ Advances in packaging technology
    - ❖ Availability of system-on-a-chip (SOC) products, which could be easily called assemblies
  - Changing landscape: With column grid arrays (CGAs), screening is no longer practical (e.g., fixturing and potential damage to the parts)

Burn-in (Contd.)

- **No clear interpretation** any longer
  - o Varied implementation
- **Periodic, frequent updates are needed!**

- **Recent Activities**
  - o At the request of NASA, the Aerospace Corporation and others, a Task Group was formed to provide guidance.
  - o More rigorous assessment is being done during audits and specification reviews pending guidance from the task group
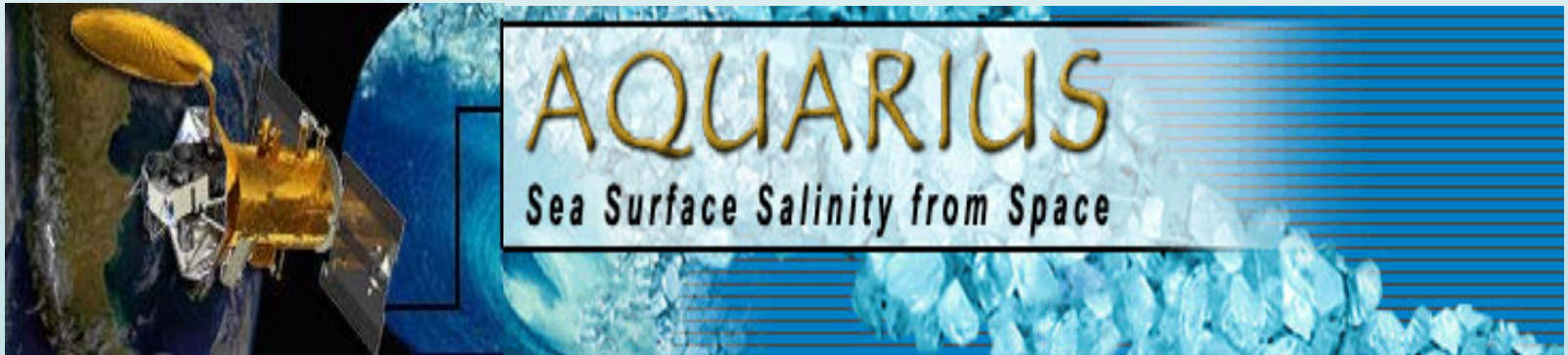
Launched June 10, 2011, the Aquarius/SAC-D mission is a partnership between NASA and Argentina's space agency (CONAE) using advanced technologies to make global space-based measurements of ocean salinity.

Microcircuits
Moving with the Times

- **NASA Class Y experience:**
  - NASA-led new technology infusion
    - A new way to conduct business
    - Supplier offered a product of system-on-a-chip (SOC) complexity,
      - ❖ of great interest to hardware designers
    - It represented advances in packaging, smaller feature sizes
      - ❖ Flip-chip, CGA. 65nm-90nm feature sizes.
    - But, it didn't fit any of the existing categories
      - ❖ So, a new Class Y was introduced
    - It also made us realize that we had reached an unchartered area
      - ❖ somewhere near the boundary of parts and boards
    - Suppliers and space community had considerable discussion on developing requirements for Class Y (some of which would apply to Class V).
    - Examples of new requirements put in 38535K:
      - ❖ Post column attach electricals (Screening)
      - ❖ Package integrity demonstration test plan, PIDTP (QCI)
    - The concept of doing screening and qualification testing remained intact

Infusion of New Technology into MIL Standards
Qualifying New Packaging Technology

- **Issue**

  - How to address the manufacturability, test, quality, and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications?

- **Proposal**

  - Each manufacturer to develop a **P**ackage **I**ntegrity **D**emonstration **T**est **P**lan (PIDTP).
  - Addresses issues unique to non-hermetic construction and materials, such as potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, thermo-mechanical stresses, & shelf life.
  - The PIDTP shall be approved by the qualifying activity after consultation with the space community. Ref: 38535K, Para B.3.11

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Infusion of New Technology into MIL Standards
Applicability of the PIDTP

- **The Package Integrity Demonstration Test Plan (PIDTP) requirement would apply to:**

    - Non-hermetic packages (e.g., Class Y). Ref: 38535K, H.3.4.4.1.1.
    - Flip-chip assembly. Ref: 38535K, H.3.4.4.1.2.
    - Solder terminations. Ref: 38535K, H.3.4.4.1.3.

- **Microcircuits employing more than one of above technologies shall include elements for each in the PIDTP.**

    Ref: 38535K, H.3.4.4.1.

NASA-Led Class Y Development

- **Looking Ahead for Class Y:**

    o Space community to work with DLA to
    - ❖ Qualify Xilinx V-4 / V-5 CN package per newly released 38535K.
        - ➢ **Xilinx announced at the SPWG that CN will be offered with Six Sigma columns**
    - ❖ Schedule QMLY audit of Xilinx and other front runners (and their supply chains)
    - ❖ Certify suppliers for column attach service per 38535K
    - ❖ Monitor on-going JEDEC task group activities (common to QMLV and QMLY)

    o Continue telecons with industry (as needed)
    - ❖ To review Class Y offerings from Xilinx, Aeroflex and e2V

Dual Use Technology

- Basically an infusion of commercial microcircuits into DoD system.
  - Building parts on commercial foundries, e.g. the use of domestic and overseas foundries by Aeroflex.
  - Adding their unique processing steps to the existing processes, e.g. MRAMs being offered by Honeywell (collaboration with Everspin)
  - Upscreening selected products from commercial portfolio (Analog Devices)

- This has resulted in paradigm changes, a couple of examples:
  - Not all parts are specified over the full military temperature range, -55C to +125C. These differences are now clearly shown in the standard microcircuit drawings (SMDs).
  - Supply chain management issues. More and more processing steps are being out-sourced. NASA and the rest of the Space community have been working with DLA to ensure the audit and approval of all entities in such supply chains.

- So, dual use technology as currently implemented by the manufacturers can be looked upon as an informed infusion of COTS into DoD standards.

- A new JEDEC issue reported:
  - Non-uniform distribution of heat across the die
  - Using thermal imaging to look for "hot spots."

Microcircuits
Thermal Resistance, Junction-to-Case

- **Hot Spots/Thermal Resistance (Theta) Junction-to-Case**
  - Affects thermal analyses at various levels (burn-in, part, board, system)
  - Recent data shows the Theta numbers are much higher than those in MIL-STD-1835.
    - ❖ MIL-STD-1835 was done a long time ago
    - ❖ Numbers were based on average temperatures across the die surface
      - ➤ Still valid for hot spots, new technology ?
  - One manufacturer is already using higher numbers in their SMDs
  - Preliminary NASA/JPL data on samples from another manufacturer shows
    - ❖ Higher Theta numbers than those given in MIL-STD-1835
    - ❖ With the part biased in a static condition, there was one hot spot on die surface. Theta varied with supply voltage.
    - ❖ With the part biased in a dynamic condition, there were additional hot spots on die surface
    - ❖ Data review in progress
  - For newer devices, a fresh approach is needed on
    - ❖ Theta computation
    - ❖ Gaining an understanding of hot spots
      - ➤ How relevant are they?
      - ➤ Static versus dynamic condition; effect of frequency, supply voltage, etc.

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Microcircuits
Screening vs Qualification

- **Summary:**

  - The baseline of performing screening followed by qualification testing has been a norm and supported by the space community and the part manufacturers:
    - ❖ Screening and qualification are inter-woven; they complement each other.

  - We have learned that the automotive parts do not get any conventional screening. But their volumes are much higher than the size of a typical NASA procurement. However, NEPP/NEPAG evaluation of automotive microcircuits is in progress. The results will be reported in future meetings.

  - At NASA, the parts requirements are defined at Center-level and project-level, such as in EEE-INST-002 and MSFC-STD-3012.
    - ❖ The requirements may have to be tailored to accommodate project needs

  - NASA is supporting (and sometimes leading the way) to infuse new technology into DoD standards. In order to ensure quality/reliability, new requirements are negotiated between the space community and the suppliers. For example, the addition of post column electricals in screening flow and PIDTP for QCI.
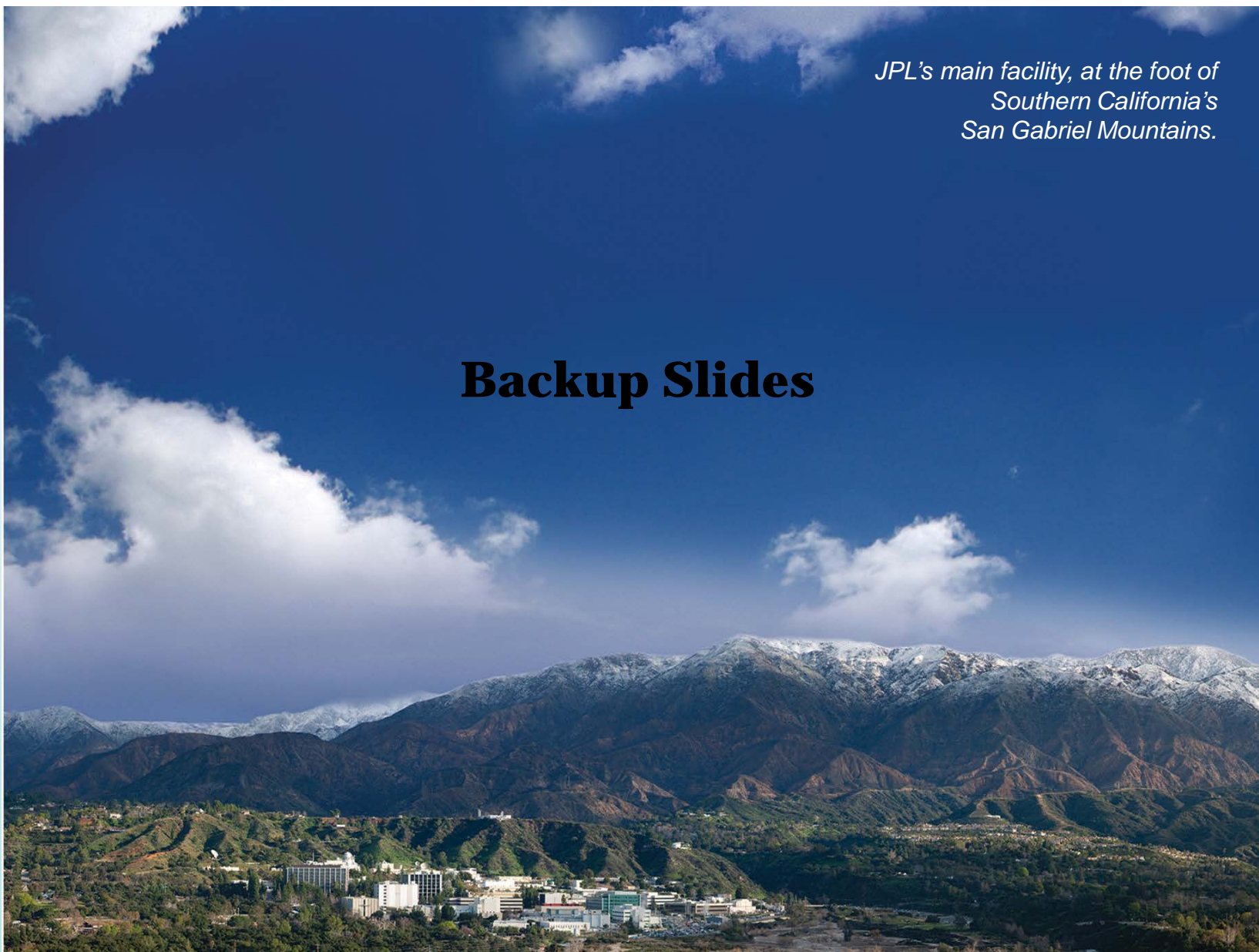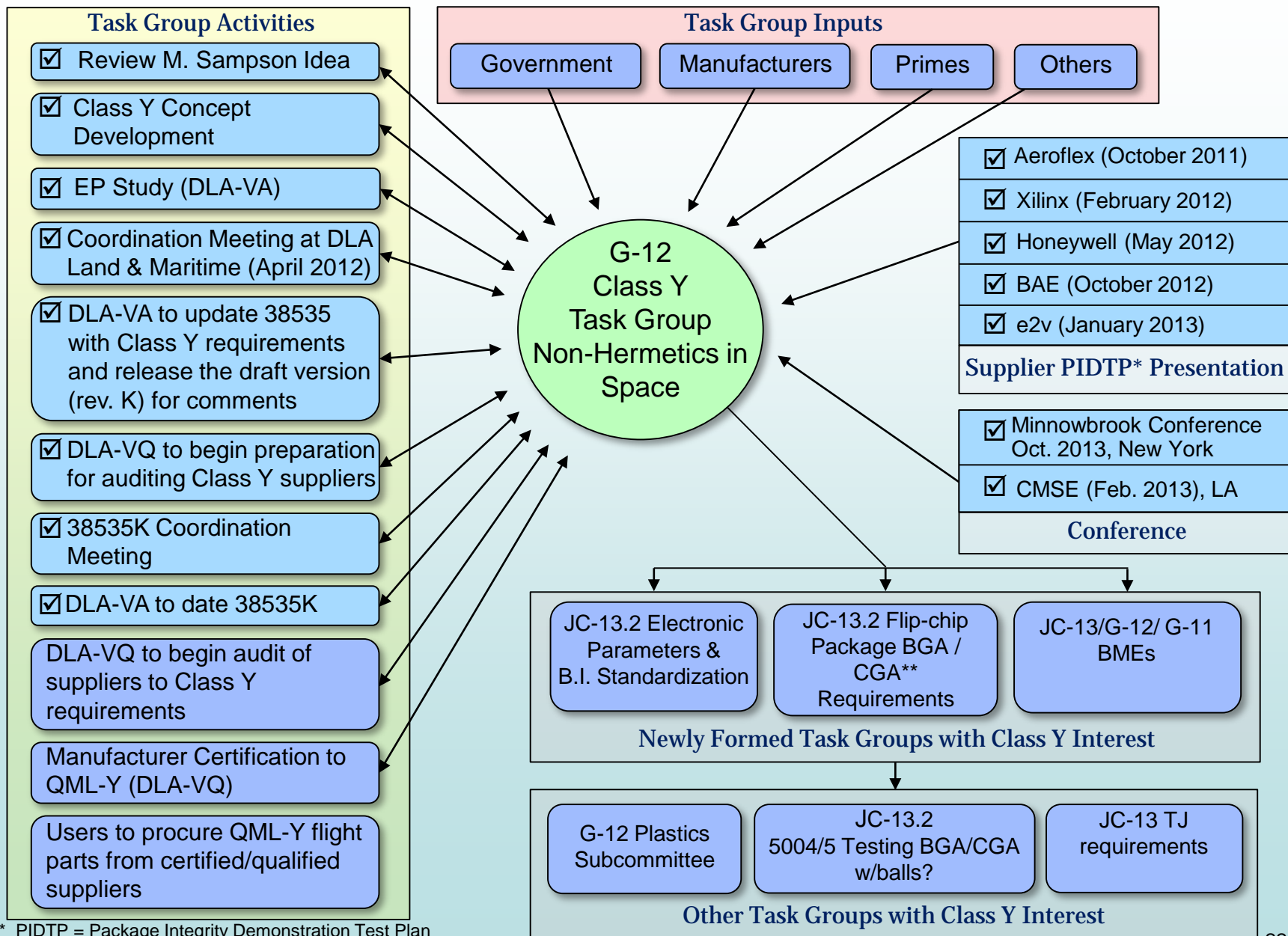
Backup Slides

JPL's main facility, at the foot of Southern California's San Gabriel Mountains.

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Infusion of New Technology into the QML System
G12 Class Y Effort at a Glance

Task Group Activities
- ☑ Review M. Sampson Idea
- ☑ Class Y Concept Development
- ☑ EP Study (DLA-VA)
- ☑ Coordination Meeting at DLA Land & Maritime (April 2012)
- ☑ DLA-VA to update 38535 with Class Y requirements and release the draft version (rev. K) for comments
- ☑ DLA-VQ to begin preparation for auditing Class Y suppliers
- ☑ 38535K Coordination Meeting
- ☑ DLA-VA to date 38535K
- DLA-VQ to begin audit of suppliers to Class Y requirements
- Manufacturer Certification to QML-Y (DLA-VQ)
- Users to procure QML-Y flight parts from certified/qualified suppliers

Task Group Inputs
- Government
- Manufacturers
- Primes
- Others

G-12 Class Y Task Group Non-Hermetics in Space

- ☑ Aeroflex (October 2011)
- ☑ Xilinx (February 2012)
- ☑ Honeywell (May 2012)
- ☑ BAE (October 2012)
- ☑ e2v (January 2013)

Supplier PIDTP* Presentation

- ☑ Minnowbrook Conference Oct. 2013, New York
- ☑ CMSE (Feb. 2013), LA

Conference

Newly Formed Task Groups with Class Y Interest
- JC-13.2 Electronic Parameters & B.I. Standardization
- JC-13.2 Flip-chip Package BGA / CGA** Requirements
- JC-13/G-12/ G-11 BMEs

Other Task Groups with Class Y Interest
- G-12 Plastics Subcommittee
- JC-13.2 5004/5 Testing BGA/CGA w/balls?
- JC-13 TJ requirements

* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

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CHANGING LANDSCAPE
Operating Temperature Ranges, Use Caution
(All SMD devices no longer guaranteed over full mil temp range)

DLA SMD 5962-99607:

Device type	Generic number	Circuit function	Access time
01	8Q512	512K X 8-bit rad-hard low voltage SRAM (MIL Temp)	25 ns
02	8Q512	512K X 8-bit rad-hard low voltage SRAM (Extended Temp)	25 ns
03	8Q512	512K X 8-bit rad-hard low voltage SRAM (MIL Temp)	20 ns
04	8Q512	512K X 8-bit rad-hard low voltage SRAM (Extended Temp)	20 ns
05	8Q512E	512K X 8-bit rad-hard low voltage SRAM (MIL Temp)	20 ns
06	8Q512E	512K X 8-bit rad-hard low voltage SRAM (Extended Temp)	20ns

Operating case temperature, (TC) (Device 01, 03, and 05) .... -55°C to +125°C
Operating case temperature, (TC) (Device 02, 04, and 06) .... -40°C to +125°C

(Bottom line: This SMD is implying that there may be a yield issue at low temperatures. Use caution for operation at low temperatures. Work with the manufacturer, get product test/characterization data.)
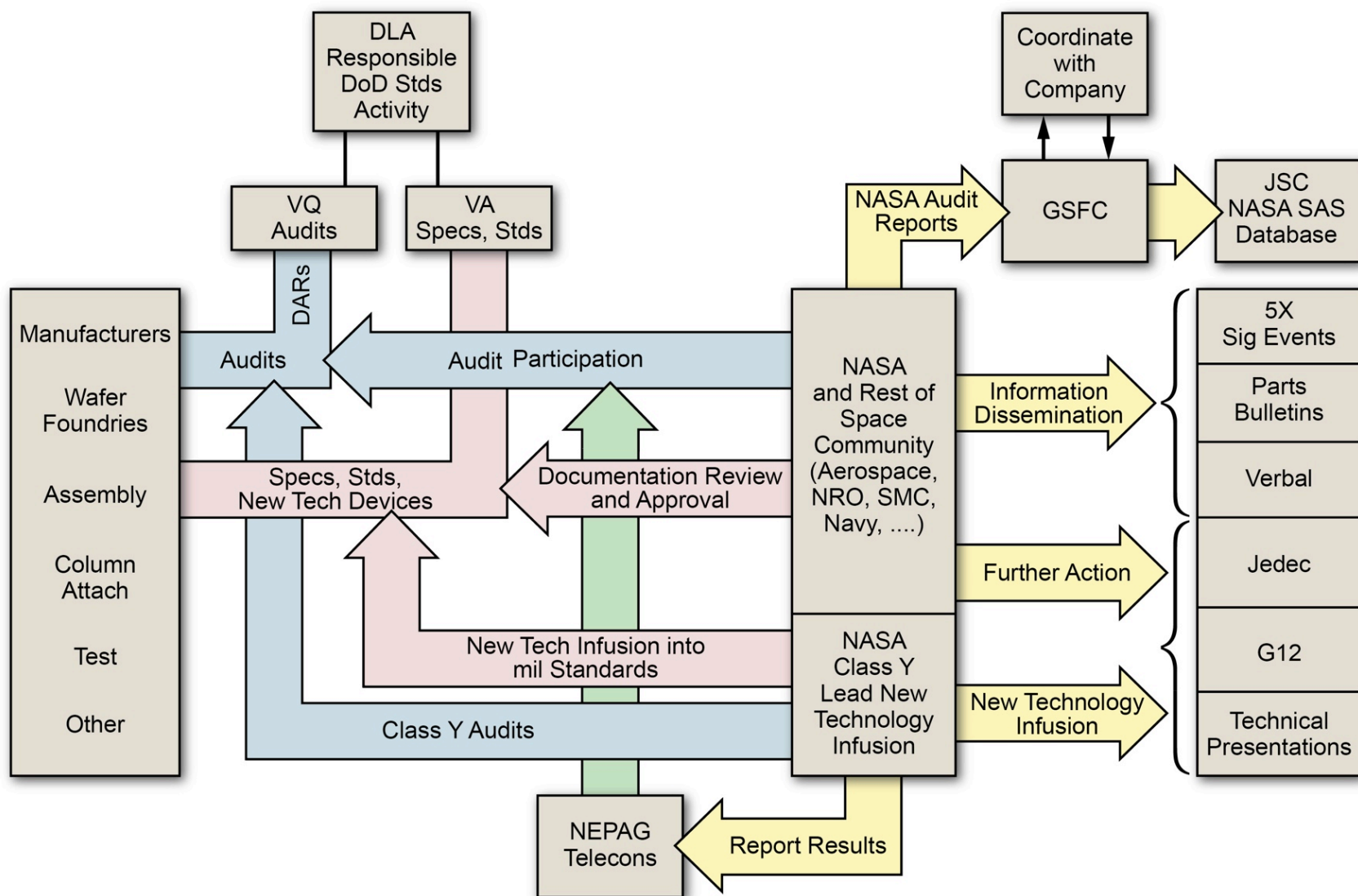
Some other examples: 5962-01533 and 5962-01511 are specified as follows:
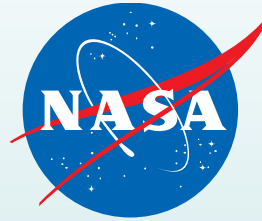**Device type 01, -40C to +125C; Device types 02 and 03, -40C to +105C.**
These may have yield problems at both low and high ends.

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Parts Standardization Activity
NEPAG/DLA/JEDEC/G12 Joint Effort

http://nepp.nasa.gov